**Logic Family**

Logic Families indicate the type of logic circuit used in the IC. The main types of logic families are:

* TTL (Transistor Transistor Logic)
* CMOS (Complementary MOS)
* ECL (Emitter Coupled Logic)

**Characteristics of Logic Families**

The main characteristics of Logic families include:

* Speed
* Fan-in
* Fan-out
* Noise Immunity
* Power Dissipation

**Speed:** Speed of a logic circuit is determined by the time between the application of input and change in the output of the circuit.

**Fan-in:**  It determines the number of inputs the logic gate can handle.

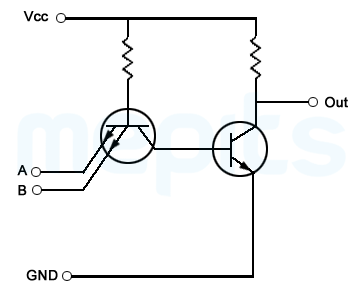
**Fan-out:** Determines the number of circuits that a gate can drive.

**Noise Immunity:** Maximum noise that a circuit can withstand without affecting the output.

**Power:** When a circuit switches from one state to the other, power dissipates.

**TTL Logic**

In transistor-transistor logic (TTL) , logic gates and other digital circuits are made using [**bipolar junction transistors**](https://www.mepits.com/tutorial/25/Transistors/Bipolar-Junction-Transistor)and resistors. The term transistor-transistor is because both logic function and amplification is done by transistor. Using TTL logic families, many [**logic gates**](https://www.mepits.com/tutorial/28/Digital-Electronics/Logic-Gates) can be fabricated in a single [**integrated circuit**](https://www.mepits.com/tutorial/123/Electronics-Devices/Integrated-Circuits). For logic gate built using TTL logic families, inputs are given to the emitters of the input transistor. In TTL logic family, analog value from 0 V to 0.8 V is logic 0 and 2 V to 5 V is logic 1. Advantages of the TTL logic families include high switching speed (125 MHz), less noise and more current (3 mA) driving capability.



**Two input NAND gate using TTL**

Figure shows TTL NAND gate. There are two transistor stages in the circuit, a multi-emitter input transistor and output transistor. Function of a multi-emitter transistor is same as that of a two parallel transistor with common base and collector terminals.

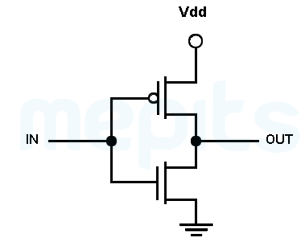
**Operation of TTL NAND Gate**

When the two emitters of the input *transistors* are connected to high voltage, then emitter-base junction of the transistor is reverse biased that means, transistor is in reverse active mode. In reverse active mode, less magnitude current flows in the opposite direction. This current reaches base of the output transistor, allowing it to conduct and pulling down the output voltage to zero. When any one of the input terminal is low, the current through other branch flows out through this terminal. Now no current reaches the base terminal of the output transistor, so output remains at high state.

**Emitter Coupled Logic (ECL)**

Emitter Coupled Logic (ECL), also referred to as **Current Mode Logic families**, is a digital technology with extremely high-speed. Transistors are not allowed to go into *deep saturation* thus, eliminating storage delays like in TTL logic families. Transistors are driven either in cut off or in active region. This is achieved by using voltage values close to each other.  For logic one it is -0.9 and for logic zero, it is -1.75v. In the active region, charge stored in the base region of transistors is kept to minimum.

Difference between these two logic states is very small. This improves the speed of operation at the expense of noise margin. Propagation time for an ECL gate is 0.5 to 2ns, which is very less when compared to its TTL counterpart.  But the disadvantage of ECL logic families is that it uses a negative power supply such that the logic levels are not compatible with any other logic family and makes analysis and measurement inconvenient. ECL logic families requires large currents therefore power dissipation is 3 to 10 times higher than that of TTL logic families. Because of its large *power consumption* and high requirement of silicon area, CMOS logic gates are preferred over ECL logic families in large scale integrated circuits.

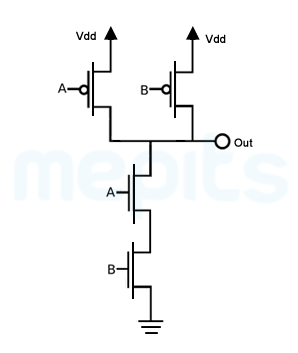


**CMOS logic**

Because of high noise immunity and low static power dissipation, now CMOS logic families is most preferred in large scale integrated circuits. CMOS (Complementary Metal Oxide Semiconductor) has complementary and symmetrical NMOS and PMOS transistors. Figure shown below is a **CMOS inverter.**

Depending on the input value, only one transistor of the CMOS inverter will be ON at a time. So in both states, there is no direct connection between power supply and ground, thereby reducing static power loss of a transistor.

**Two input CMOS NAND gate**

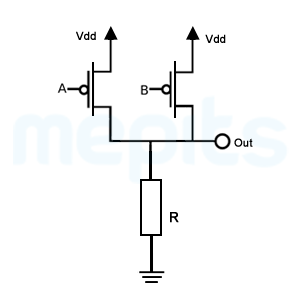


When both inputs of a **CMOS NAND gate** are at high, then transistors T1, T2 will be ON and transistors T3, T4 will be OFF. Now there is a direct connection between output and ground through transistor T3 and T4. Output is pulled down to zero.

When any of the input is low, either transistor T3 or T4 will be off. This breaks the connection between output terminal and ground. At the same time, one of the PMOS transistors is ON, so there is connection between output and power supply. Now output is pulled up to logic high.

**PMOS logic**

The structure of **PMOS logic** can be obtained by replacing NMOS transistors in the CMOS Circuit by a *pull down resistor*. Operation of a PMOS logic family can be explained by considering a PMOS NAND gate.

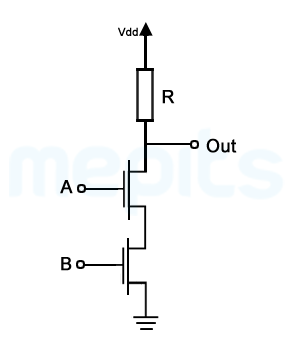


**Two input PMOS NAND**

When logic low is applied to either A or B, the corresponding transistor will be turned ON. This makes a direct connection between power supply and output terminal. Now the output is raised to logic high value. In other cases output will remain at logic low (pulled down by the pull-down resistor).

**NMOS logic**

NMOS logic is similar to that of PMOS logic. Instead of PMOS here we use **NMOS transistor** along with a *pull up resistor*. NMOS is preferred over PMOS and CMOS logic families because of its speed and easiness in the manufacturing. When output is at logic low, static power dissipation is very high. So in application requiring minimum static power dissipation, NMOS logic is replaced by CMOS logic.



**Two input NMOS NAND**

A two input **NMOS NAND gate** has two NMOS transistor connected in series from the output to ground terminal and a pull-up resistor from output terminal to power supply. When both inputs are at logic high, both transistors will be ON establishing a connection between output terminal and ground. Thus output is pulled down to ground voltage. When any one the input is at logic high then the transistor will be OFF, cutting off the path between output terminal and ground. Thus output will remain at high voltage, pulled up by the pull-up resistor.